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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,163	10/02/2000	Jerry D. Kline	1303-1008	4116

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/25/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,163	KLINE, JERRY D.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The objection to drawings is withdrawn in response to applicant's amendment filed 4/17/02.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Razon et al. (US 6,136,681).

Razon et al. identically teach the claimed method comprising the steps of :

- electrically and mechanically coupling a semiconductor wafer 100 having a plurality of integrated circuit chips 100a/100b/100c etc. to an interposer 106 to form a wafer-interposer assembly as shown in Fig. 2B;
- simultaneously testing multiple integrated circuit chips 100a/100b/100c etc. of the semiconductor wafer 100, i.e. the text on col. 4, lines 41-42 Razon et al. state that "

prior to the integration of the devices 101, each chip on wafer 100 is testing using conventional electrical test equipment" and the test is simultaneously performed on the multiple chips 100a/100b/100c etc. since the teaching is performed on a wafer-level integration (col. 2, line 66 through col. 3, line 3 and col. 4, lines 29-30);

- dicing the wafer-interposer assembly into a plurality of chip assemblies using cutting blade 114 as shown in Fig. 2F (col. 6, lines 55-57);

- selecting at least two of the chip assemblies corresponding to the multiple integrated circuit chips for inclusion in the matched set based upon the testing, i.e. selecting those integrated circuit chips which comply with the electrical acceptance criteria for the matched set based upon the testing and marked those defective chips as mis-matched set which may be discarded followed by the dicing step (col. 4, lines 42-55). The steps of testing and selecting of Razon et al. also inherently teaches the limitations as specified in claims 2-6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam (US 6,281,046) in view of the admitted prior art in the instant invention (pp. 2-4).

Lam teaches the claimed method comprising the steps of :

- electrically and mechanically coupling a semiconductor wafer 21 having a plurality of integrated circuit chips 25 to an interposer 31 to form a wafer-interposer assembly 39 (figs. 1, 5, 6; col. 4, lines 61-62; col. 5, lines 13-19);
- simultaneously testing at least two of the integrated circuit chips 25 of the semiconductor wafer 21 (col. 5, lines 19-20), i.e. multiple chips 25 are on the single wafer 21 but are not diced until the packaging operation (e.g. testing, solder alignment, etc.) on the single wafer 21 has been completed (col. 3,lines 19-22); and the interposer substrate 31 can be approximately the same size as the wafer 21 and is coupled to the wafer 21 (col. 4, lines 53-54), i.e. when multiple chips 25 are under testing they are tested at the same time because multiple chips 25 are on the single wafer 21 and are tested before they are diced into plural chip assemblies 70 and 72; and then
- dicing the wafer-interposer assembly 39 into a plurality of chip assemblies such as 70 and 72 (col. 5, line 24-26).

Lam does not expressly teach selecting at least two of the chip assemblies for inclusion in the matched set based upon the testing.

Applicant's admitted prior art, however, teaches that in order to enhance the overall packaging performance it usually requires a selecting step by matching chips having similar behavior as a matched set (page 3, second paragraph of the specification).

Therefore, it would have been obvious to the ordinary skilled art in the art to comprise the selecting step of admitted prior art after the dicing step of Lam to select at least two chip

assemblies for inclusion in the matched set based upon the testing results since by doing so it would enhance the overall packaging operation.

Regarding claims 2-6, Lam does not expressly the purposes of testing. Applicant's admitted prior art, however, teaches that in order to improve overall electronic device performance a matched set is used and the testing is carried out, wherein the testing step includes testing chips together to identify which groups of chips perform best together for inclusion (page 2, last paragraph through page 3, line 1); testing chip compatibility; testing chips over a range of temperature (page 3, second paragraph); and the IC chips of the semiconductor wafer can be RF devices (page 3, second paragraph).

Therefore, it would have been obvious to the ordinary skilled art in the art to include the testing items as taught by the admitted prior art in Lam's testing step in order to improve the device performance.

Regarding claims 7-13 and 24-30, the Examiner takes an official notice that they are routine check items during the testing step.

Regarding a matched set as recited in claim 36, Lam' method also inherently teaches the claimed matched set, which includes a substrate onto which two chip assemblies are electrically coupled (Figs. 1, 5, 6 and related text).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee
June 18, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800